AMENDMENTS TO THE CLAIMS

Claims 1-29 (canceled)

30. (currently amended): A pixel circuit comprising:

a photodetector that generates charge;

a storage node for receiving charge generated by said photodetector;

an amplifier having an input coupled to said storage node and an output that provides an amplified input signal, said amplifier having a first power mode during a first operational period and a second power mode during a second operational period;

a feedback capacitor, said capacitor providing feedback between the amplifier's output and input; and

a reset switch that resets said storage node when closed.

31. (original): The circuit of claim 30 further comprising a transfer transistor that transfers said charge from said photodetector to said storage node and a switch for selectively connecting one of a first and second power source to said amplifier.

32. (original): The circuit of claim 31, wherein an output power of said second power source is greater than an output power of said first power source.

33. (canceled)

34. (original): The circuit of claim 30, wherein said storage node is a floating diffusion node separate from said photodetector.

35. (original): The circuit of claim 30, wherein said reset switch resets said feedback capacitor when closed.

36. (original): The circuit of claim 33, wherein said reset switch resets said photodetector from a reset voltage line when closed.

37. (original): The circuit of claim 30 further comprising a select switch, said select switch connecting the amplifier output to a column line when closed.

38. (original): The circuit of claim 30, wherein an output stage of said amplifier resides outside of a pixel array.

39. (original): The circuit of claim 30, wherein said amplifier is configured as a folded four-transistor cascode amplifier.

40. (original): The circuit of claim 34 further comprising a transfer transistor that transfers said charge from said photodetector to said amplifier.

41. (original): The circuit of claim 39 further comprising a switch circuit that connects a pixel to a column line.

42. (original): The circuit of claim 30 further comprising a reset transistor that resets said photodetector and said feedback capacitor.

43. (currently amended): An integrated circuit comprising:

a pixel array with rows and columns of pixel cells, and, for each column, a column readout line that connects to the column's pixel cells; each pixel cell including:

a photodetector that provides a first signal indicating detected light;

an amplifier with an input that receives the first signal and an output that provides an output signal based on the first signal, said amplifier having a first power mode during an integration period and a second power mode during a readout period; and

feedback capacitance that provides feedback from the amplifier output to the amplifier input; and

readout circuitry connected to the column readout line, the readout circuitry providing readout signals from the column pixel cells; the readout circuitry including sampling circuitry for sampling the amplifier output signal.

44. (original): The integrated circuit of claim 43 in which each pixel cell further comprises a transfer transistor that transfers said charge from said photodetector to said amplifier.

45. (original): The integrated circuit of claim 43, wherein said amplifier selectively receives a reset signal and a charge generated signal at an input, said sampling circuitry obtaining a reset sample and a charge signal sample from said amplifier output.

46. (original): The integrated circuit of claim 43, in which the amplifier and feedback capacitor form a capacitive transimpedance amplifier.

47. (original): The integrated circuit of claim 43 in which the amplifier includes an input transistor and an output stage.

48. (original): The integrated circuit of claim 43 in which the amplifier is a single ended four-transistor cascode amplifier.

49. (original): The integrated circuit of claim 48 further comprising a transfer transistor that transfers said charge from said photodetector to said amplifier.

50. (original): The integrated circuit of claim 43, wherein the readout circuitry further includes amplifier output stage circuitry; when each pixel cell is connectable to a column line, the amplifier and the output stage circuitry forming a distributed amplifier.

51. (original): The integrated circuit of claim 43 in which each pixel cell further comprises a switch for selectively connecting one of a first and second power source to said amplifier.

52. (currently amended): An integrated circuit comprising:

a pixel array with rows and columns of pixel cells and, for each column, a column readout line that connects to pixel cells of a column; each pixel cell including:

a photodetector that provides a first signal indicating detected light;

an amplifier with an input that receives the first signal and an output that provides signals based on the first signal, said amplifier having a first power mode during a first operational period and a second power mode during a second operational period; and

feedback capacitance that provides feedback from the amplifier output to the amplifier input; and

readout circuitry connected to the column readout line, the readout circuitry providing readout signals from a column line; the readout circuitry including:

amplifier output stage circuitry arranged such that when the pixel cell is connected to a column line the amplifier and the output stage circuitry form a distributed amplifier.

53. (original): The integrated circuit of claim 52 in which the output stage circuitry is outside the pixel array.

54. (original): The integrated circuit of claim 52 in which the pixel array further includes select circuitry that connects a pixel cell to an associated column readout line in response to a row select signal.

55. (original): The integrated circuit of claim 52, wherein said distributed amplifier is configured as a single ended four-transistor cascode amplifier.

56. (original): The integrated circuit of claim 52, wherein said distributed amplifier is configured as a folded four-transistor cascode amplifier.

57. (original): The integrated circuit of claim 52 wherein said distributed amplifier is configured as a differential input telescopic cascode amplifier.

58. (original): The integrated circuit of claim 52 further comprising a transfer transistor that transfers said charge from said photodetector to said amplifier.

59. (original): The integrated circuit of claim 58, wherein said distributed amplifier is configured as a single ended four-transistor cascode amplifier.

60. (original): The integrated circuit of claim 58, wherein said distributed amplifier is configured as a folded four-transistor cascode amplifier.

61. (original): The integrated circuit of claim 58 wherein said distributed amplifier is configured as a differential input telescopic cascode amplifier.

62. (original): The integrated circuit of claim 52, wherein said photodetector senses visible light.

63. (original): The integrated circuit of claim 52, wherein said photodetector senses infrared light.

64. (original): The integrated circuit of claim 52 in which each pixel cell further includes a reset switch that, when closed, resets the photodetector to a reset level.

65. (original): The integrated circuit of claim 52 in which each pixel further includes a reset switch that, when closed, resets the photodetector and the amplifier to a reset level.

66. (original): The integrated circuit of claim 52 in which each pixel further includes a reset switch that, when closed, resets the amplifier and a floating diffusion node coupled to the photodetector and to the input of said amplifier.

67. (original): The integrated circuit of claim 52 in which the readout circuitry further includes a sampling circuit connected to said column readout line.

68. (currently amended): An imaging circuit comprising:

an array of pixels, each pixel including:

a photodetector that generates charge in response to light;

a storage node for storing charges generated by said photodetector;

an amplifier that amplifies a signal received from said storage node, said amplifier having a first power mode during a operational period and a second power mode during a second operational period;

a feedback capacitor that provides feedback to an input of the amplifier; and

a reset switch that resets a storage node when closed~~; and~~.

69. (original): The circuit of claim 68, wherein said amplifier is a capacitive transimpedance amplifier.

70. (original): The circuit of claim 68, wherein at least a portion of said amplifier is located outside said array of pixels.

71. (original): The circuit of claim 68 in which the array further comprises, for each pixel cell, a first select switch that connects said capacitor and said reset switch to the amplifier output circuit when closed.

72. (original): The circuit of claim 68 in which the array further comprises, for each pixel cell, a second select switch that connects the amplifier input to the amplifier output circuit when closed.

73. (original): The circuit of claim 68 in which the array further comprises, for each pixel, a transfer transistor that transfers charge from said photodetector to said amplifier.

74. (original): The circuit of claim 68, wherein said amplifier is a distributed amplifier configured as a folded four-transistor cascode amplifier.

75. (currently amended): A pixel sensor array comprising:

an array of pixel cells, each pixel cell including:

a photodetector that generates charge in response to light;

an amplifier that amplifies a signal received from said photodetector, said amplifier having a first power mode during an integration period and a second power mode during a readout period;

a feedback capacitor that provides feedback to the input of the amplifier; and

a reset switch that resets the photodetector from a reset voltage line when closed.

76. (original): The array of claim 75 in which each pixel cell further comprises a transfer transistor that transfers charge from said photodetector to said amplifier.

77. (currently amended): An imaging system comprising:

a processor;

an imaging device coupled to said processor, the imaging device comprising:

an array of pixels, each pixel including:

a photodetector that generates charge in response to light;

a storage node for storing charges generated by said photodetector;

an amplifier that amplifies charges on said storage node, said amplifier having a first power mode during an integration period and a second power mode during a readout period;

a feedback capacitor that provides feedback to an input of the amplifier; and

a reset switch that resets the storage node when closed; and

amplifier output circuitry located outside the pixel array; the amplifier, the amplifier output circuitry, and the feedback capacitor together forming a capacitive transimpedance amplifier.

78. (original): The system of claim 77 in which each pixel further comprises a first transfer transistor that transfers charge from said photodetector to said storage node.

79. (original): The system of claim 77 in which the imaging device further comprises a sampling circuit that samples the output of said amplifier.

80. (original): The system of claim 77, wherein said capacitive transimpedance amplifier is configured as a single ended four-transistor cascode amplifier.

81. (original): The system of claim 77, wherein said capacitive transimpedance amplifier is configured as a folded four-transistor cascode amplifier.

82. (original): The system of claim 77, wherein said capacitive transimpedance amplifier is configured as a differential input telescopic cascode amplifier.

83. (canceled)

84. (original): The system of claim 77, wherein said storage node is a floating diffusion node separate from said photodetector and said reset switch resets said floating diffusion node when closed.